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(12) United States Patent

Yamaguchi et al.

(54) POWER SEMICONDUCTOR DEVICE

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(56) References Cited

U.S. PATENT DOCUMENTS

4.689.871 A 9/1987 Malhi

(Continued)

FOREIGN PATENT DOCUMENTS

10-163483 6/1998

JP

(Continued)

OTHER PUBLICATIONS

Mitsuhiko Kitagawa et al., "A 4500 V Injection Enhanced Insulated Gate Bipolar Transistor (EGT) Operating in a Mode Similar to a Thyristor" IEDM 93-679, 1993, pp. 59-62.

(Continued)

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(57) **ABSTRACT**

A power semiconductor device includes trenches disposed in a first base layer of a first conductivity type at intervals to partition main and dummy cells, at a position remote from a collector layer of a second conductivity type. In the main cell, a second base layer of the second conductivity type, and an emitter layer of the first conductivity type are disposed. In the dummy cell, a buffer layer of the second conductivity type is disposed. A gate electrode is disposed, through a gate insulating film, in a trench adjacent to the main cell. A buffer resistor having an infinitely large resistance value is inserted between the buffer layer and emitter electrode. The dummy cell is provided with an inhibiting structure to reduce carriers of the second conductivity type to flow to and accumulate in the buffer layer from the collector layer.

17 Claims, 25 Drawing Sheets

